Design full adder with multiplexers



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Making of the XOR

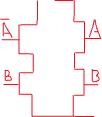


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The pull-down network:



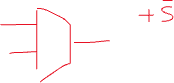
For pull up networks, we need the complementary expression.



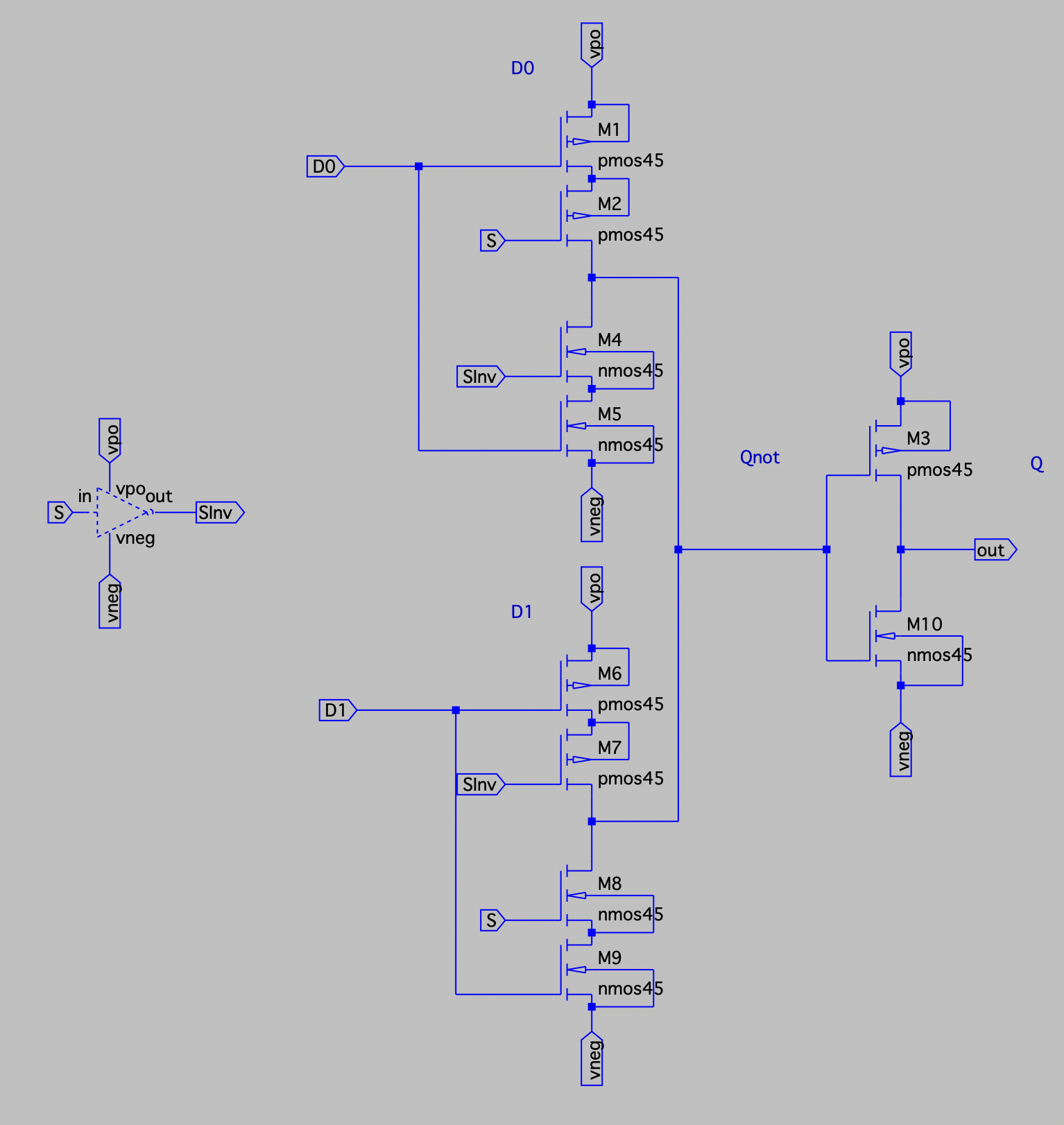
Multiplexer design

|  |  |  |  |
| --- | --- | --- | --- |
| S | D0 | D1 | Y |
| 0 | 0 | X | 0 |
| 0 | 1 | X | 1 |
| 1 | X | 0 | 0 |
| 1 | X | 1 | 1 |

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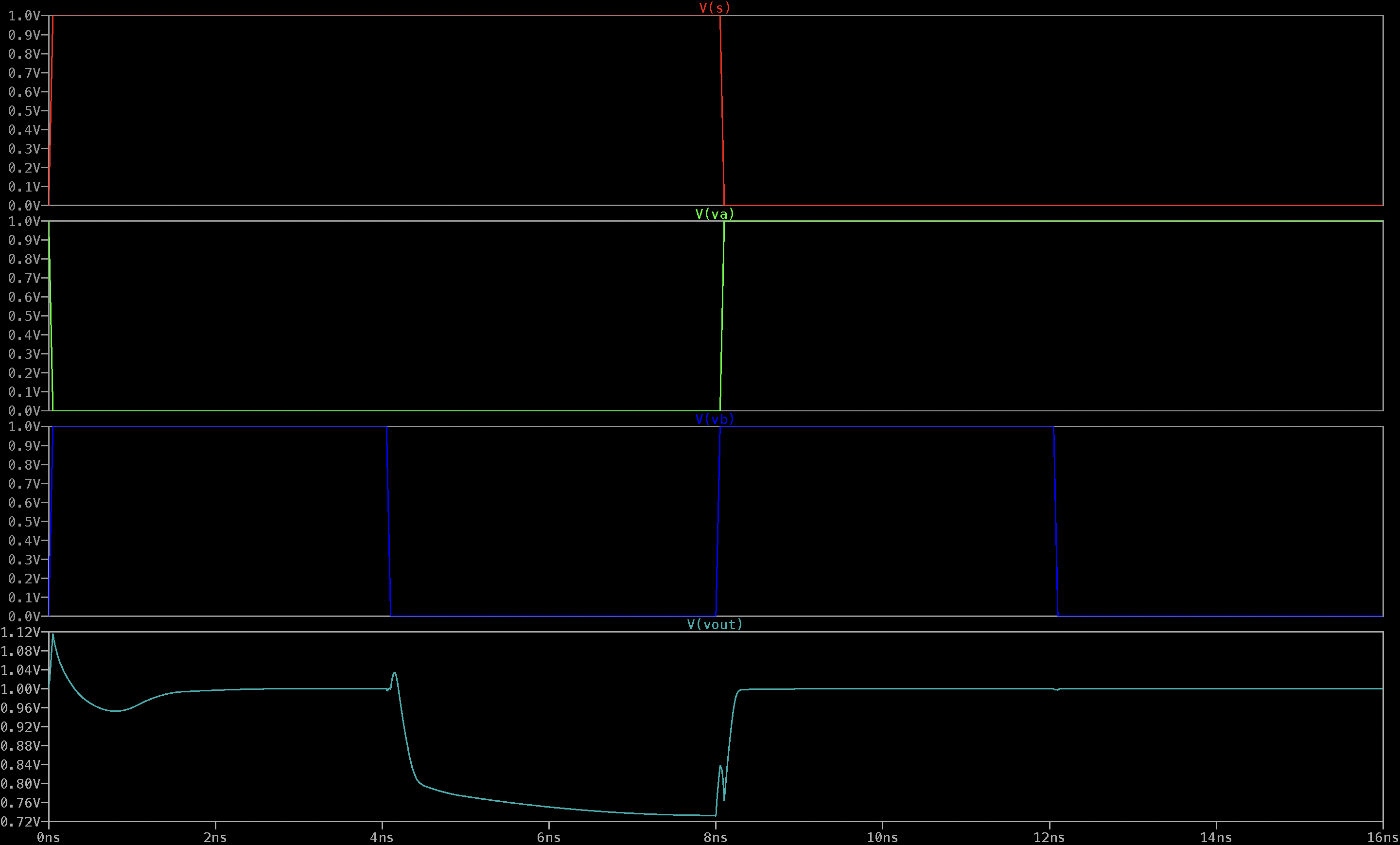
The design I use comes from a previously shown design from our lectures.

Et billede, der indeholder diagram, tekst, Plan, Teknisk tegning

Automatisk genereret beskrivelseThen making it to the following subcircuit:

Figure : Multiplexer designed in ltspice

Figure : Multiplexer design from class

Equaling the following analysis: 

Which shows it isn’t ideal, but works as a multiplexer, with S being 1 at start, choosing the vb voltage, and then S switches to 0, choosing the voltage of va.

Now I have made the subcircuits, and then only missing putting them together to make a full adder.

We have derived the full adder ourselves in the past, so I won’t be doing that again. The outputs of the full adder is known to be:

The design comes to be the following in LTSpice.

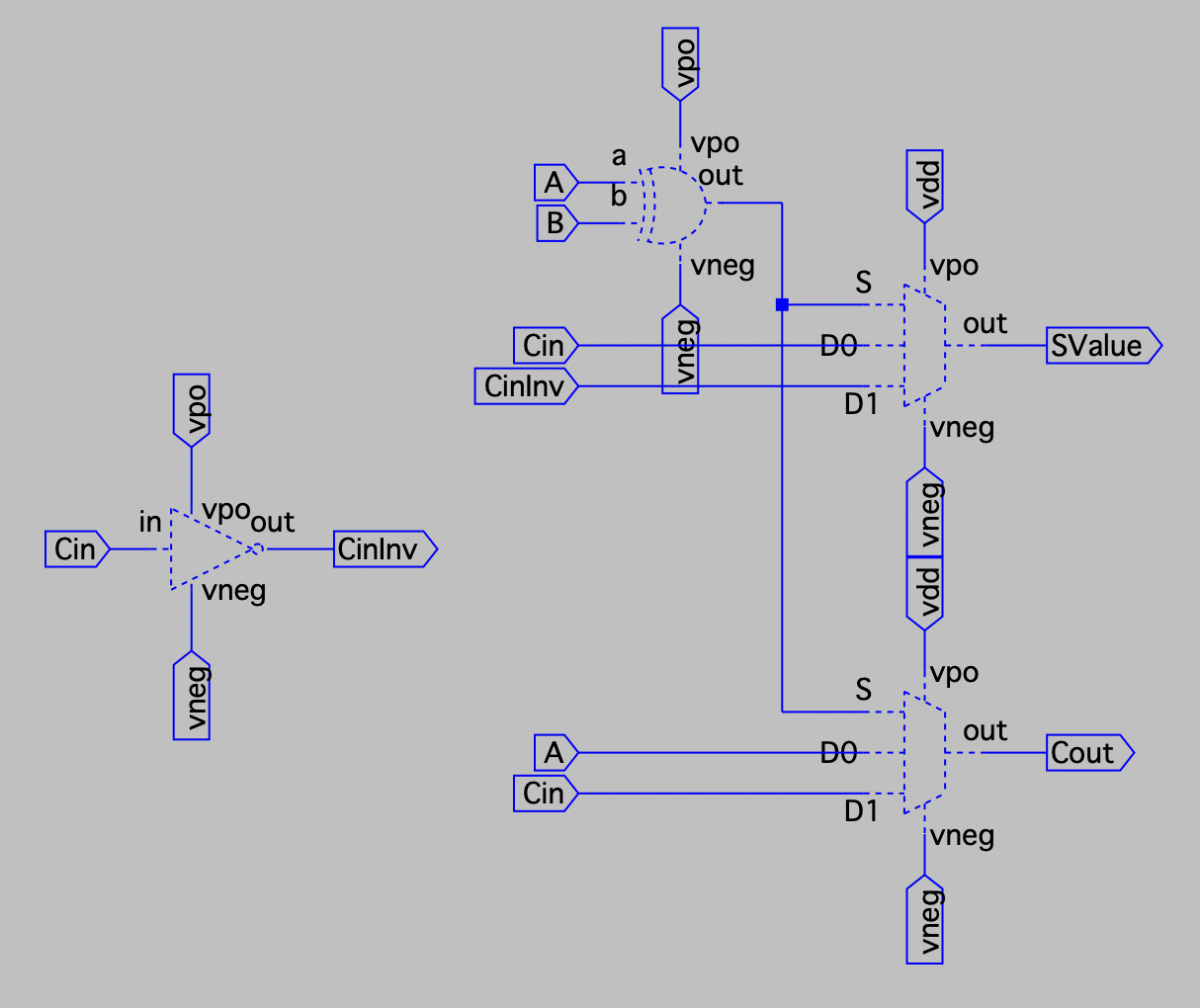
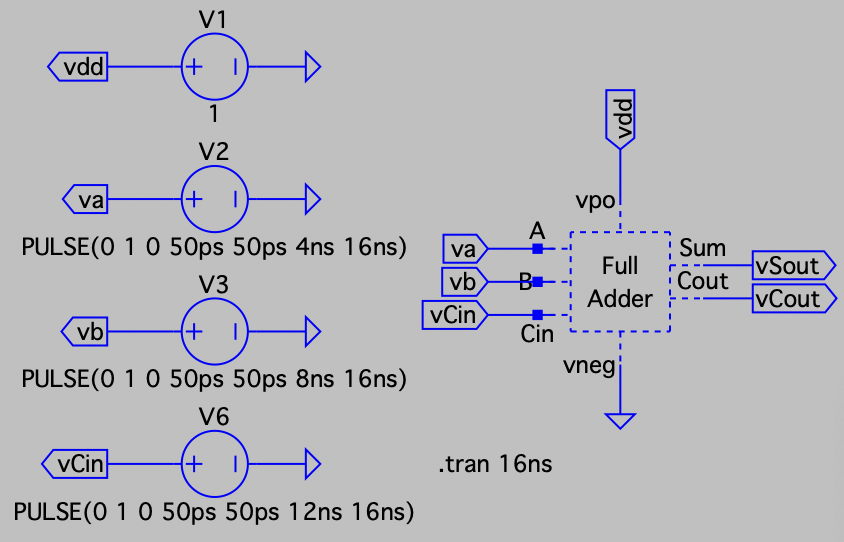
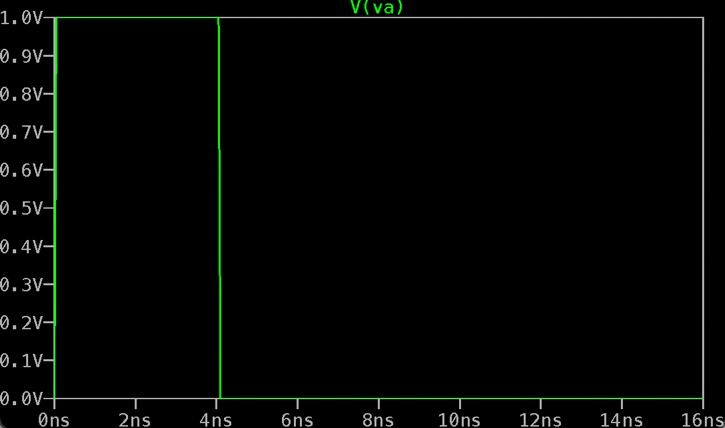


Figure 3: Full adder design in LTSpice

Making a symbol for it, and then testing it. The test schematic:



Resulting in:



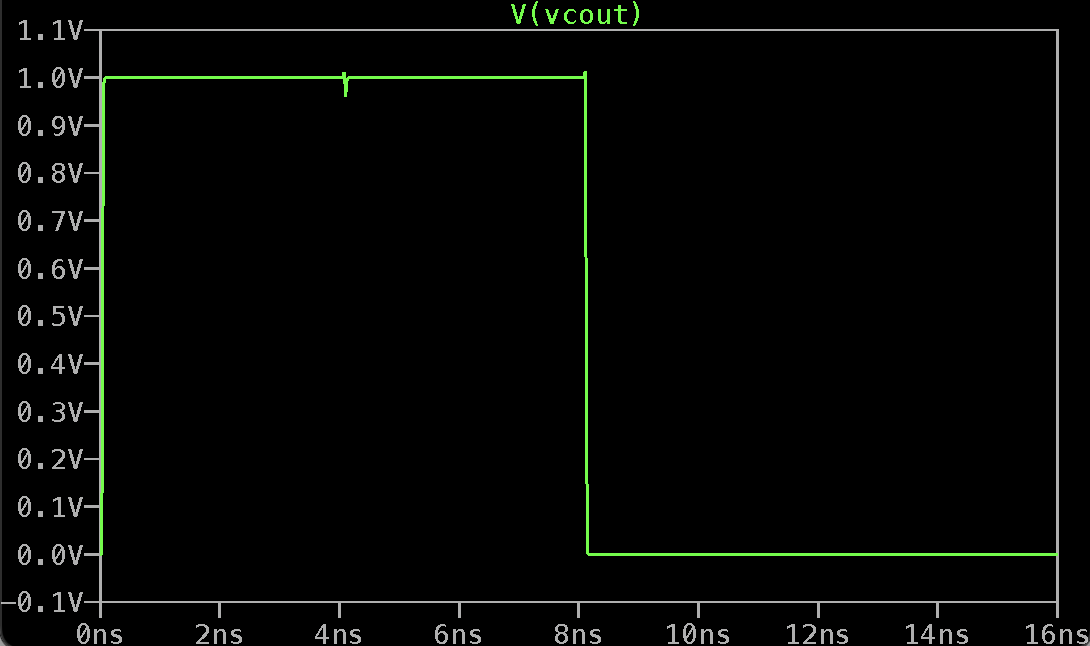
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Et billede, der indeholder skærmbillede, tekst, Kurve

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 Et billede, der indeholder skærmbillede, tekst, Grafiksoftware

Automatisk genereret beskrivelse

My simulation chose to interpret the counting backwards, but that’s alright.

Starting from 3 and counting down to 0.

Looking at C being 1, and S being 1, this checks out √.

Looking at C being 1, and S being 0, this checks out √.

Looking at C being 0, and S being 1, this checks out √.

Looking at C being 0, and S being 0, this checks out √.

So now I have gotten a schematic for a working full adder made from a circuit using some Multiplexers, a XOR and some Inverters, all using CMOS technology.